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TWO-DIMENSIONAL NUMERICAL SIMULATION OF NEGATIVE DIFFERENTIAL MOBILITY SEMICONDUCTING DEVICES

By
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and
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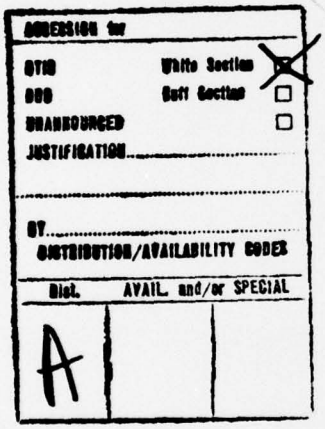
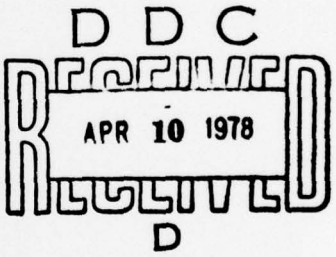
The simulation is implemented using interactive computer graphics. As the solution evolves, displays of the potential, charge density and current flow in the semiconductor are available via a computer graphic terminal. Sample results of simulations of a negative differential mobility field effect transistor are presented.





TWO-DIMENSIONAL NUMERICAL SIMULATION OF NEGATIVE DIFFERENTIAL MOBILITY SEMICONDUCTING DEVICES

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ABSTRACT

A numerical simulation in two spatial dimensions of negative differential mobility semiconducting devices is described. The simulation models time dependent operation of two or three terminal devices in an external circuit.

The mathematical model of the semiconductor consists of a set of nonlinear second-order partial differential equations which are solved on a rectangular mesh using explicit finite difference techniques. The external circuit is modeled using lumped linear elements and the resulting equations are solved using implicit techniques. The external circuit equations are coupled to the semiconductor equations by the current flow and potential at the device terminals. The solution of the resulting time dependent boundary value problem is a feature of the simulation which permits more realistic numerical analysis of NDM devices than was previously possible.

The simulation is implemented using interactive computer graphics. As the solution evolves, displays of the potential, charge density and current flow in the semiconductor are available via a computer graphic terminal. Sample results of simulations of a negative differential mobility field effect transistor are presented.

INTRODUCTION

A field effect transistor (abbreviated FET) is a device in which the bulk conductance of an extrinsic semiconductor is controlled by an externally applied bias. Several mechanisms may be used to achieve this control; one of which employs a reverse bias Schottky contact to control the cross-sectional area through which current flows. A principal feature of FET operation is that it is a majority carrier effect. The minority carriers do not effectively participate in transistor action.

One possible configuration of an FET is shown in Fig. 1. The device consists of an n-type semiconductor with low resistance contacts at either end, labelled source and drain. On the top of the semiconductor is a Schottky metal electrode, called the gate contact, which has the effect of creating a region that is relatively free of mobile carriers (shaded region). The region beneath the depleted region contains the mobile carriers and is called the conducting channel. The device generally sits atop of a semi-insulating substrate, and may be separated from it by a buffer layer.

In normal FET operation the source and drain contacts are connected by an external circuit and primary current flows through the conducting channel. The width of the depleted region, and consequently that of the conducting channel, is determined by the potential within the channel. The potential within the channel is dependent on both the gate and drain potential and the dc resistance is, therefore, bias dependent. Typical source-drain current-voltage characteristics are therefore nonlinear and dependent on the gate potential (1).

With the exception of very recent work most analyses of FET devices, e.g., amplifiers, are small signal studies. The starting point for these studies is the known dc distribution of space charge, electric field and voltage within the device. Theoretical studies usually involve two-dimensional approximations to the three-dimensional structure, and can be grouped into either analytical or numerical approaches. The analytical studies, which include the original proposal of Shockley (1), generally consist of reducing the complicated two-dimensional analysis to a series of separate but connected one-dimensional problems. The analysis permits calculations of the current-voltage characteristics, the transconductance, etc., from which parameters for device design can be extracted.

The postulated space charge distribution within an FET determines how the device is designed for a specific application. The adequacy of the analytical studies for determining the space charge distribution has been scrutinized carefully as inconsistencies between theory and experiment have emerged. In one general study, using numerical techniques, Kennedy et al. (2) predicted that, at sufficiently high bias values, regions of carrier accumulation and depletion would form within the conducting channel of the device; a phenomenon not predicted by earlier analytical studies. The presence of these nonuniform space charge layers was shown to affect the gate bias dependence of the primary current-voltage characteristics.

Within the past few years considerable activity has centered around the semiconductors gallium arsenide and indium phosphide as FET materials. While InP is of recent interest, GaAs FET's provide the prospect of linear amplification of microwave signals of up to at least 10 GHz, output power of several watts and a bandwidth of an octave or more. From the point of view of device design it is recognized that the space charge distribution within this material is nonuniform and in some cases electrically unstable (3). The reason for the latter is that for long conducting channels and sufficiently high fields the electrons may acquire enough energy to become 'hot' and create a region of negative differential mobility where the average mobility decreases with increasing electric field, see Fig. 2. If the latter occurs the device becomes electrically active and introduces a mechanism that competes with the small signal operation of the device; namely, the spontaneous nucleation and subsequent propagation of local regions of high electric fields (Gunn domains).

The prospect of dealing with electrically active semiconductors introduces additional constraints in FET design. In the first place low resistance contacts are known to allow the formation of Gunn domains. In certain cases instabilities associated with these domains can be eliminated. In other cases, as in logic applications, Gunn domain nucleation and propagation are features incorporated into the design of the device. The time dependent behavior of electrically active semiconductors cannot always be described by small signal time dependent analyses. The nature of the problem dictates that the transient phenomena be treated in as realistic a way as is

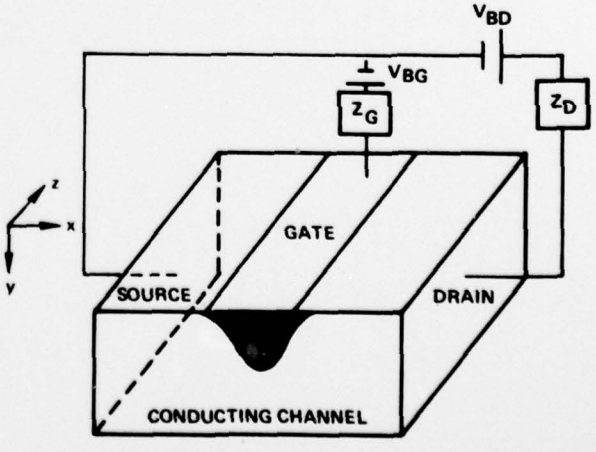

Fig. 1. An FET configuration with source and drain contacts on the ends of the device and the gate contact on top. The device is modeled in the xy plane.

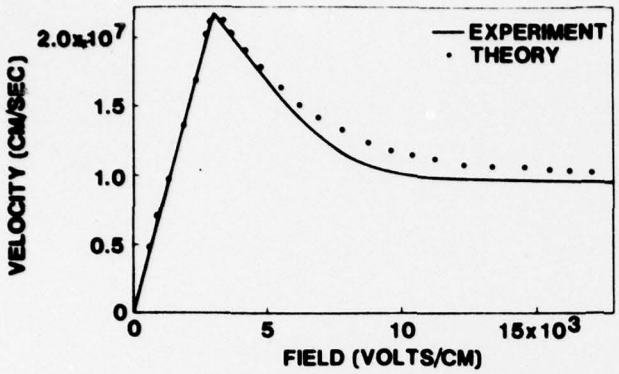

Fig. 2. The velocity versus electric-field v(E) curve for n-GaAs. The theoretical curve is that of Butcher-Fawcett (6) and the experimental points were obtained by Ruch-Kino (7).

numerically possible. Accurate modeling of GaAs FET's demands large signal time dependent analysis in at least two dimensions.

Large signal transient analysis of FET's has been done for time independent potential on the contacts (4,5). An initial device state is chosen which is incompatible with the final steady state and the resulting transient relaxation is then studied. A more difficult but more realistic problem is solved in this paper in which the semiconductor equations and the external circuit equations are solved and coupled together through time dependent boundary conditions, specifically the contact potentials.

The principal approximations in the mathematical formulation are (a) the three-dimensional carrier flow is reduced to two dimensions by assuming the variables to be independent of the z coordinate, and (b) all minority conduction is ignored. Within this framework a numerical simulation of field dependent mobility devides is performed. The mathematical model of the semiconductor consists of a set of nonlinear partial differential equations which are solved on a rectangular mesh using explicit finite difference techniques. Particular attention is paid to the selection of boundary conditions. The boundary conditions approximate the physical and electrical characteristics of the outer periphery of the semiconductor structure. The exposed surfaces of the semiconductor are assumed to be ideal electrical insulators; and no current is permitted normal to these bounding surfaces. The low resistance contacts and the gate contact are approximated by equipotential surfaces with a prespecified charge density. For the calculations illustrated, the low resistance source and drain contacts are charge neutral and located sufficiently far from the active region of the device so that for the current levels involved they have no influence on the electrical properties of the device. A specific impurity atom distribution is assumed, which in general can be spatially dependent. In the sample calculations it is assumed to be homogeneous.

The semiconductor equations are coupled to the circuit equations by the boundary conditions at the device terminals. The solution of the resulting time dependent boundary value problem is a feature of the simulation and represents an advance in the state-of-the-art of these types of calculations.

The simulation is implemented using interactive computer graphics. As the solution evolves, displays of the potential, charge density and current flow in the semiconductor are available via a computer graphics terminal.

FORMULATION

The relevant semiconductor equations for unipolar two-dimensional electron conduction include Poisson's equation

$$\nabla^2 V(x,y,t) = \frac{e}{\epsilon}\left[N(x,y,t) - N_0(x,y,t)\right] \tag{1}$$

and

$$\vec{E}(x,y,t) = -\text{grad } V(x,y,t) \tag{2}$$

for carriers of charge -e where $e = 1.6\text{x}10^{-19}$ coul. ϵ is the permittivity of the material which, for GaAs is $9.8\text{x}10^{-3}$ coul^2/joule-cm. $V(x,y,t)$ is the potential, $\vec{E}(x,y,t)$ the electric field, $N(x,y,t)$ the mobile carrier density, and $N_0(x,y,t)$ the position dependent background doping density. For the sample calculations N_0 is a constant equal to $10^{15}/\text{cm}^3$.

The average electron velocity is related to the electric field through the relation

$$\vec{w}(x,y,t) = -\mu(|\vec{E}|)\vec{E}(x,y,t) \tag{3}$$

where $\vec{w}(x,y,t)$ is the average electron velocity and $\mu(|\vec{E}|)$ is the field dependent mobility.

The equation for carrier transport including diffusion is

$$\vec{j}(x,y,t) = eN(x,y,t)\mu(|\vec{E}|)\vec{E}(x,y,t) + e\text{Dgrad } N(x,y,t) \tag{4}$$

where D is the diffusion coefficient, which is generally electric field dependent. In the sample calculations, D is taken to be constant and equal to 200 cm^2/sec. The above equations are subject to the constraints of the equation of continuity

$$\text{div } \vec{j}(x,y,t) = e\frac{\partial}{\partial t}\left[N(x,y,t) - N_0(x,y,t)\right] \tag{5}$$

or

$$\text{div } \vec{i}(x,y,t) = 0 \tag{6}$$

where

$$-\vec{i}(x,y,t) = \vec{j}(x,y,t) + \frac{\epsilon\partial\vec{E}(x,y,t)}{\partial t} \tag{7}$$

The boundary conditions to the above equations are derived from the surface and contact properties: no current flows through the free surfaces. With the assumptions of zero permittivity for the surrounding space, this leads to

$$\hat{n}\cdot\text{grad } V = \hat{n}\cdot\text{grad } N = 0 \tag{8}$$

along the free surfaces. $\hat{n}$ is a unit vector normal to the free surface of the semiconductor. At the source, drain and gate contact $N(x,y,t)$ is preassigned. For the sample calculations

$$N_{source} = N_{drain} = N_O = 10^{15}/cm^3 \tag{9}$$

and

$$N_{gate} = 10^{-3} N_O \tag{10}$$

The source potential is set to zero and the gate potential V_G and drain potential V_D are determined by simultaneous solution of the semiconductor equations and the circuit equations.

For the three contact device of Fig. 1 the circuit equations are

$$V_S = 0 \tag{11}$$

$$V_{BD}(t) = I_D(t)Z_D + V_D(t) \tag{12}$$

$$V_{BG}(t) = I_G(t)Z_G + V_G(t) \tag{13}$$

$$I_S(t) = I_G(t) + I_D(t) \tag{14}$$

where V_S is the source potential, V_G the gate potential, V_D the drain potential, I_S the source current, I_G the gate current, I_D the drain current, Z_G the gate impedance, Z_D the drain impedance. The external circuit impedances are modeled as lumped linear elements. The current passing across a contact is the integral over the contact area of the component of current density normal to the contact. For a device of dimension, ℓ_z, in the z direction, and a contact extending over a region, ℓ,

$$I(t) = \ell_z \int_{\ell} \hat{n} \cdot \vec{J}(x,y,t)\, d\ell' \tag{15}$$

The loop currents and external circuit potentials are normalized with respect to the peak average electron velocity for GaAs and the corresponding electric field, respectively. The loop currents and circuit impedances are further normalized with respect to the device depth, ℓ_z.

The sign of the current density, $\vec{J}$, as well as the signs of the loop currents in the external circuit are consistent with conventional current flow. In particular, for the circuit of Fig. 1, positive source current, I_S, implies electron flow into the device at the source contact and positive drain current, I_D, implies electron flow out of the device at the drain contact. Positive gate current, I_G, implies electron flow out of the device at the gate contact.

DIFFERENCE EQUATIONS

The device potential and mobile carrier density are computed on a uniform rectangular mesh. The mesh contains LxM internal nodes with boundary conditions imposed via additional nodes at the edges of the device. Therefore, the total number of nodes, including the boundary, is (L+2)x(M+2). Derived quantities such as electric field, charge and total current densities are defined at points other than the nodes although they are written in terms of the nodal indices. Let ℓ be the index in the y direction, m the index in the x direction, and X the uniform mesh increment. Let k be a time index and T the time increment.

Poisson's equation is discretized using the five point formula

$$V_{k,\ell+1,m} + V_{k,\ell-1,m} + V_{k,\ell,m+1} + V_{k,\ell,m-1} - 4V_{k,\ell,m} = X^2 \frac{e}{\epsilon} (N_{k,\ell,m} - N_{O_{k,\ell,m}}) \tag{16}$$

$$1 \le \ell \le L$$
$$1 \le m \le M$$

The boundary potentials $V_{k,o,m}$, $V_{k,L+1,m}$, $V_{k,\ell,o}$, $V_{k,\ell,M+1}$ are determined from Dirichlet conditions on the contacts and Neumann conditions elsewhere. The potential on the contact is found by solution of the external circuit equations. Away from the contact the normal electric field is assumed to be zero on the boundary.

The components of electric field are defined between nodal points as follows:

$$E_{x_{k,\ell,m}} = -\frac{(V_{k,\ell,m} - V_{k,\ell-1,m})}{X}$$
$$E_{y_{k,\ell,m}} = -\frac{(V_{k,\ell,m} - V_{k,\ell,m-1})}{X} \tag{17}$$

As defined above $E_{x_{k,\ell,m}}$ is located midway between the nodes $(\ell-1,m)$ and (ℓ,m), while $E_{y_{k,\ell,m}}$ is located midway between nodes $(\ell,m-1)$ and (ℓ,m). In order to compute the mobility, $\mu(|\vec{E}|)$, an average electric field $\vec{E}_{(av)}$ is calculated whose x and y components are

$$E_{x(av)_{k,\ell,m}} = 0.5\,(E_{x_{k,\ell,m}} + E_{x_{k,\ell,m-1}})$$
$$E_{y(av)_{k,\ell,m}} = 0.5\,(E_{y_{k,\ell,m}} + E_{y_{k,\ell-1,m}}) \tag{18}$$

The vector $\vec{E}_{(av)}$ thus computed is located in the center of a square which has at its corners the nodes (ℓ,m), $(\ell-1,m)$, $(\ell,m-1)$, $(\ell-1,m-1)$. Numerical experiments have indicated that the method of computation of $\vec{E}_{(av)}$ affects the stability of the solution. Other methods which have been reported (4,5) lead to more complex or less stable algorithms than Eq. (18). The average electron velocity is computed from $\vec{E}_{(av)}$ as follows:

$$\vec{w}_{k,\ell,m} = -\mu(|\vec{E}_{(av)}|)\vec{E}_{(av)_{k,\ell,m}} \tag{19}$$

so that $\vec{w}$ is defined at the same location as $\vec{E}_{(av)}$. A specific velocity-electric field curve is included in the simulation via a piecewise linear map of mobility versus electric field magnitude. The carrier transport equation is

$$j_{x_{k,\ell,m}} = \frac{-e(N_{k,\ell,m} + N_{k,\ell-1,m})(w_{x_{k,\ell,m}} + w_{x_{k,\ell,m+1}})}{4} + \frac{eD}{X}(N_{k,\ell,m} - N_{k,\ell-1,m}) \qquad 1 \le \ell \le L+1,\ 1 \le m \le M$$
$$j_{y_{k,\ell,m}} = \frac{-e(N_{k,\ell,m} + N_{k,\ell,m-1})(w_{y_{k,\ell,m}} + w_{y_{k,\ell+1,m}})}{4} + \frac{eD}{X}(N_{k,\ell,m} - N_{k,\ell,m-1}) \qquad 1 \le \ell \le L,\ 1 \le m \le M+1 \tag{20}$$

The charge current density, $\vec{j}$, is defined such that $j_{x_{k,\ell,m}}$ is located midway between nodes (ℓ,m) and $(\ell-1,m)$ and

$j_{y_{k,l,m}}$ is located midway between nodes (l,m) and (l,m-1).

An explicit integration formula is used to propagate the mobile carrier density in time:

$$N_{k+1,l,m} = N_{k,l,m} + \frac{T}{eX}\left(j_{x_{k,l+1,m}} - j_{x_{k,l,m}} + j_{y_{k,l,m+1}} - j_{y_{k,l,m}}\right) \tag{21}$$

$$1 \le l \le L$$

$$1 \le m \le M$$

where N_0 has been assumed to be time independent.

The total current density, $\vec{i}$, is calculated so that its components are defined at the same locations as the charge current density:

$$i_{x_{k,l,m}} = -j_{x_{k,l,m}} - \frac{\epsilon}{T}\left(E_{x_{k+1,l,m}} - E_{x_{k,l,m}}\right)$$

$$1 \le l \le L+1$$

$$1 \le m \le M$$

$$i_{y_{k,l,m}} = -j_{y_{k,l,m}} - \frac{\epsilon}{T}\left(E_{y_{k+1,l,m}} - E_{y_{k,l,m}}\right) \tag{22}$$

$$1 \le l \le L$$

$$1 \le m \le M+1$$

The total current on each contact is found by integrating the normal component of total current density over all nodes associated with the contact.

The external circuit equations are solved using an implicit scheme. For resistive circuit elements

$$V_{D_k} = V_{BD_k} - R_D \cdot I_{D_k}$$

$$V_{G_k} = V_{BG_k} - R_G \cdot I_{G_k} \tag{23}$$

where R_D is the drain circuit resistance and R_G is the gate circuit resistance.

Method of Solution

The presence of the external circuit introduces some difficulties into the solution of the equations describing the device charge distribution. The difference equations have been derived assuming time independent boundary potential. Referring to Eq. (22), unless the boundary potential at time k+1 is the same as the boundary potential at time k, the current density will not be correctly computed. In particular, the current density in the region of the contacts will not satisfy Eq. (6); that is, it will not be divergence free. The difficulty is overcome by the use of the following artifice: the mobile carrier density is propagated forward in time by a small increment, $T' < T$, over which it is sufficiently accurate to assume that the boundary potential does not change. Let $N_{k+\delta}$ be the mobile carrier density which has been propagated by T'. Then propagation to the next full time step is performed as follows:

$$N_{k+1,l,m} = N_{k,l,m} + \frac{T}{T'}\left(N_{k+\delta,l,m} - N_{k,l,m}\right) \tag{24}$$

The solution requires initial conditions $N_{o,l,m}$, I_{G_o}, I_{D_o} and boundary conditions on V and N. At each time step the solution procedure may be summarized as follows, given $N_{k,l,m}$, $I_{G_{k-1}}$, $I_{D_{k-1}}$ and estimates of I_{G_k}, I_{D_k}:

1. Find $V_{k,l,m}$, $j_{k,l,m}$
2. Find $N_{k+\delta,l,m}$
3. Find $i_{k,l,m}$
4. Update estimates of I_{G_k}, I_{D_k}

Relaxation iteration is used to update the estimates of the total currents I_{G_k} and I_{D_k}. When the iterations have converged the mobile charge density is propagated to the next time step using Eq. (24).

The solution of the difference equations is straightforward with the exception of the discrete form of Poisson's equation, Eq. (16). Methods for the solution of Poisson's equation are summarized and compared by Dorr (8). From the available techniques direct solution by Gaussian elimination has been chosen. Gaussian elimination is not generally used when two space dimensions are involved since precomputation and storage of an LxLxM array is required. However, when the solution mesh is such that L is much less than M, as is the case with the devices being studied, and when the mesh size is not too large, Gaussian elimination, by virtue of its computational efficiency for time dependent problems, is the method of choice. The procedure for solution of the discrete Poisson's equation in two dimensions by Gaussian elimination is reviewed in (8).

Stability

Stability analysis of the device difference equations is possible only when linearizing assumptions are made. The stability of the explicit integration of Eq. (21) can be shown by von Neumann stability analysis to be limited by

$$T < \frac{X^2}{4D}\ , \quad T < \frac{D}{v^2} \tag{25}$$

when constant boundary potential and constant average electron velocity ($\vec{w} = -v$ = constant) are assumed. Typical values for GaAs are $X = 10^{-5}$ cm, $D = 200$ cm^2/sec, and $v = 10^7$ cm/sec so that the stability limit is $T < X^2/4D = 1.25\times10^{-13}$ sec. Note that for low values of diffusion, stability is limited by $T < D/v^2$. Implicit integration of carrier density has been used in simulations of silicon semiconductors which exhibit low diffusion coefficients (4). Numerical experiments have indicated, however, that for devices with field dependent mobility, $\mu(\vec{E})$, the stability criteria derived from the linearized system are of limited usefulness in predicting performance of a particular method. The sample calculations to be presented subsequently were performed at a time increment of 3.96×10^{-13} sec, and numerical stability was maintained for the same time increment when the diffusion coefficient was reduced to zero. Additional numerical experiments have shown that, for GaAs devices operating in the negative differential mobility regime, implicit integration affords no improvement in computational efficiency over explicit integration.

Analysis of the stability of the external circuit equations is possible when the eleotric field in the device is assumed to be homogeneous and of sufficiently low magnitude that average electron velocity is a linear function of electric field. When these assumptions are made the device is seen to be capacitive. Thus, when the external circuit impedances are resistors a one time step delay applied to the loop currents in the external circuit equations, which leads to an explicit expression for the boundary potentials, also leads to numerical instability. Therefore, the implicit formulas, Eq. (23), are employed. A relaxation iteration with a relaxation constant less than one (under relaxation) is used for both the gate and drain circuits (9).

SAMPLE CALCULATIONS

The simulation is demonstrated by two sample calculations presented in Figs. 3-7. The solution is found on an 8x40 mesh exclusive of boundary nodes. The configuration which is simulated is that of Fig. 1 in which the source and drain are on the sides of the device and the gate is on the top. The parameters are as follows:

device length (x)	10 microns
device width (y)	2.19 microns
X	0.244 microns
T	3.96×10^{-13} sec
gate width	3.416 microns
Z_G	0
Z_D	R_0
D	200 cm/sec^2
N_0	10^{15} cm^{-3}

where R_0 is the intrinsic low field resistance which depends on the dimensions of the device in the z direction. Given the loop current normalization with respect to device depth, it is sufficient to state that $Z_D = R_0$. The background charge density on the gate contact is set to 10^{-3} N_0. A three piece linear approximation of the velocity-electric field curve of an NDM device has been used in which the electron velocity at high field is one half the peak velocity. The source and gate potentials are zero. Realistic initial conditions are achieved by applying a small drain bias potential to the device and running the simulation until the mobile carrier density, which is initially set to N_0, reaches steady state.

Figure 3 shows the time and space evolution of the mobile carrier density and the vector distribution of current density within the FET which occur when the drain bias, V_{BD}, is ramped from 0.1 to 1.0, in normalized units, in 4 picoseconds. The left-hand column shows N(x,y,t) at successive instants of time. For clarity in the display N(x,y,t), expressed in units of N_0, increases in the downward direction. The current density displays are vector displays showing both magnitude and direction. The line segments reduce to points when the magnitude of the total current density is zero and reach their maximum length when the magnitude of the current density is greater than or equal to the peak current for GaAs (see Fig. 2). The time evolution of the loop currents and the drain potential are displayed in Fig. 4 in normalized units.

The details of the display show an evolving depletion layer that moves into the semiconductor under the gate electrode. The depletion layer, where $N(x,y,t) < N_0$, implies a transverse component of electric field pointing in the direction of the gate electrode and causing electron flow into the semiconductor through the gate. Note the current density display of Fig. 3 at 5.3 ps and also Fig. 4 where the magnitude of the gate current initially exceeds the source current. In

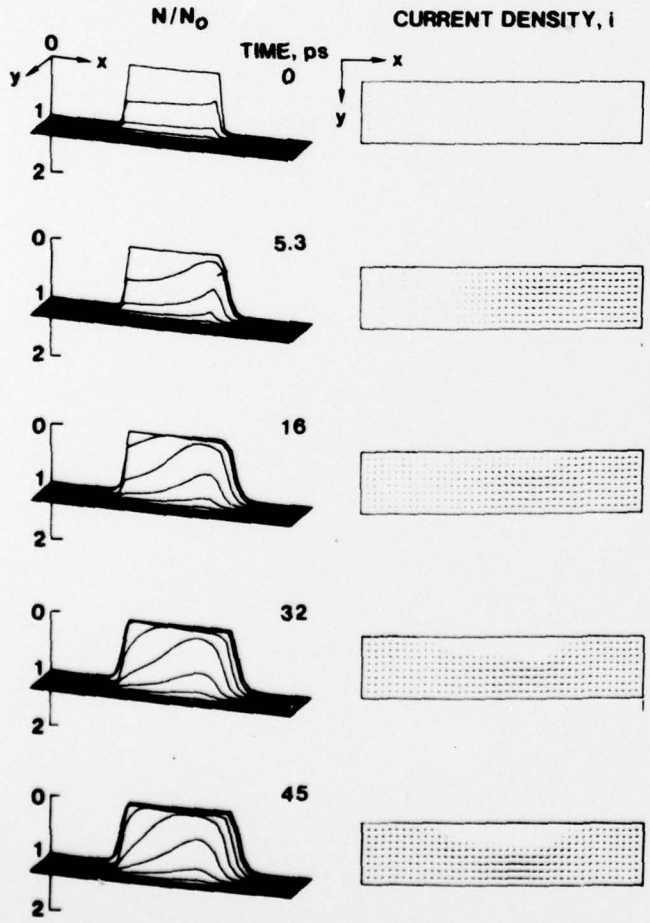

Fig. 3. The time and space evolution of the normalized mobile carrier density, N/N_0, and current density, i, which occurs when the drain bias potential is ramped from 0.1 to 1.0 in 4 ps.

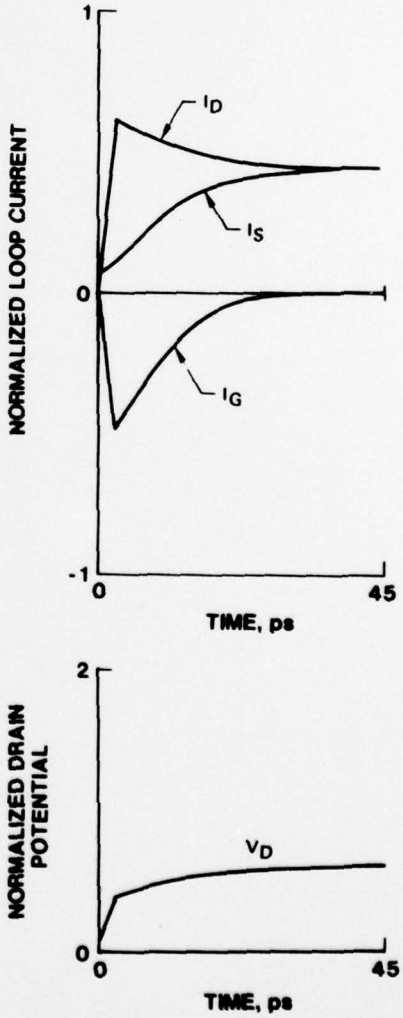

Fig. 4. The time evolution of the loop currents and drain potential when the drain bias potential is ramped from 0.1 to 1.0 in 4 ps.

steady state the gate current approaches zero. It is significant to note in Fig. 3 that the current density in steady state is greatest under the gate contact where the cross-sectional area of the conducting channel is least. For the particular set of bias potentials all field values within the conducting channel are less than the electric field at peak current for GaAs and therefore the increase in current density is accomplished without any local regions of charge accumulation.

In the second sequence, shown in Figs. 5-7, the drain bias potential is ramped from 0.1 to 2.0 while the source and gate potentials are held at zero. In the absence of a gate electrode, such a drain bias potential would not be sufficiently large to cause the device to operate in the region of negative differential mobility. However, the constriction caused by the gate electrode increases the magnitude of the electric field under the gate to a level such that the device operates locally in the NDM regime. The scale of Fig. 5 is such that the length of the line segments representing current density merge into a solid line just as the NDM regime is entered. The area in which NDM operation is initiated may be clearly seen just under the gate. An accumulation of mobile carriers occurs and, in the sequence shown in Fig. 6, moves from the gate to the drain where the accumulation decays. The process then repeats itself and will do so indefinitely. The evidence of oscillations within the device is the presence of oscillations in the loop current in the external circuit, Fig. 7. Note in Fig. 7 that the drain potential is time dependent and therefore an assumption of constant potential would not be realistic for this situation.

SUMMARY

A computer simulation has been presented which allows large signal time dependent analysis of bulk semiconductors operating in an external circuit. The simulation was developed to study negative differential mobility devices; however, any semiconducting material for which a velocity-electric field curve is known may be modeled. Although the sample calculations presented were performed for a specific contact configuration, the simulation permits placement of the contacts anywhere on the boundaries. The primary limitation of the numerical technique is that the device must be modeled on a rectangle.

By simulating the interaction of the semiconducting device and the external circuit a more representative analysis of device behavior is possible; particularly in those situations where the assumption of constant electrode potential is not valid.

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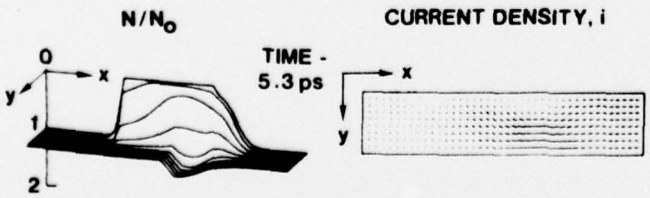

Fig. 5. The normalized mobile carrier density and current density at the initiation of an accumulation of mobile carriers.

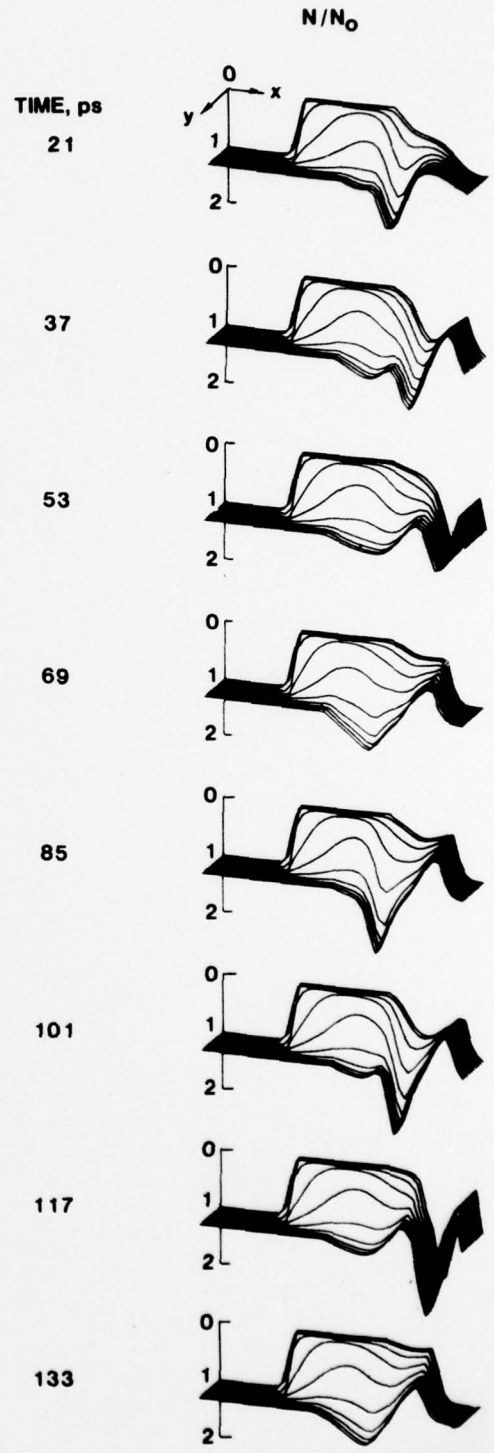

Fig. 6. A time sequence showing the formation and propagation of Gunn domains in a GaAs FET.

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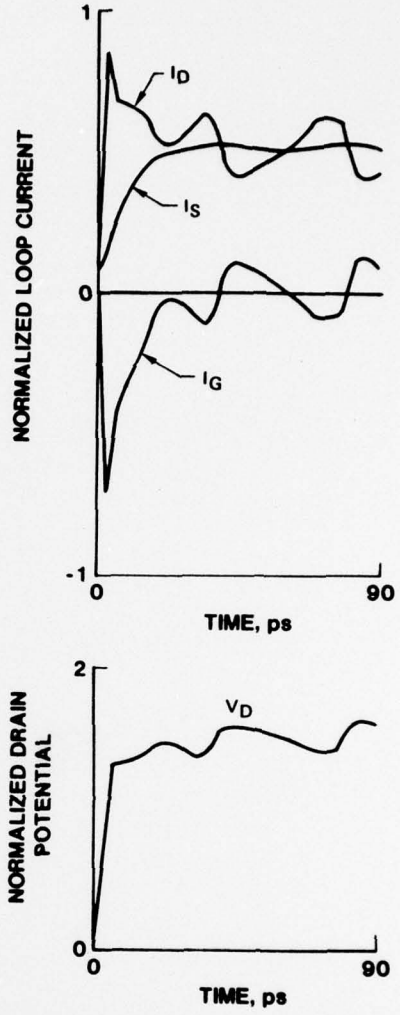

Fig. 7. The time evolution of loop currents and drain potential which occurs during Gunn type oscillations. The transient and the first cycle of the oscillation is shown.

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